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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,502	01/20/2004	Terry C. Coughlin JR.	ROC920030381US1	1485

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EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,502	COUGHLIN, TERRY C.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen [U.S. Patent #6,078,195].

As per claim 4, an AVT circuit library comprising: a plurality of hybrid AVT circuits, each said hybrid AVT circuit including a plurality of PFETs and a plurality of NFETs [column 6, lines 23-35]; each PFET having a LVT [column 4, lines 6-8, 36-37, 49-50; column 5, lines 21-23; column 6, lines 23-35]; and each NFET having a SVT [column 4, lines 6-8, 37-38, 50-52; column 5, lines 21-23; column 6, lines 23-35]. As per claim 5, wherein said hybrid AVT circuits include a corresponding SVT circuit having a LVT mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET [column 11, lines 2-18]. As per claim 6, wherein said LVT PFET is provided in an Nwell region isolated from said NFET in each said hybrid AVT circuit [column 11, lines 2-18].

Claim Rejections - 35 USC § 103

Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. [U.S. Patent #5,666,288] in view of Chen [U.S. Patent #6,078,195].

As per claims 1/7, Jones et al. teach a method/computer program product comprising the steps of: identifying circuits in a circuit library [column 1, lines 11-12; column 3, lines 29-32; column 5, lines 47-60; column 6, lines 48-57]; for each circuit, replacing each transistor to provide a hybrid circuit [column 3, lines 39-60; column 4, lines 57-61; column 5, lines 66-67; column 6, lines 37-44; column 8, lines 30-35]; and saving each said hybrid circuit in an alternate circuit library [column 3, lines 61-62; column 4, lines 57-61; column 7, lines 61-64]. However, Jones et al. do not explicitly teach SVT circuits, SVT PFETs or LVT PFETs. Chen teaches providing mixed SVT and LVT devices including PFETs and maintaining each NFET having a SVT [column 4, lines 6-8, 36-37, 49-50; column 5, lines 21-23; column 6, lines 23-35], and making a library [column 6, lines 33-

35]. Considering that Jones et al. suggest changing each transistor to accommodate voltage characteristics [column 6, lines 36-44; column 8, lines 10-12, 30-35; column 10, lines 21-30] and that Chen suggest making a library with SVT and LVT devices including PFETs and NFETs [column 6, lines 23-35], a person of ordinary skill in the art at the time of the invention would have found it obvious to combine these teaching to obviate the claimed invention because "its merits in standby power, speed and noise margin, such mixed-low-and-regular-V_t logic books can have a wide use in VLSI designs (e.g., high performance microprocessor design)" [Abstract, lines 13-16]. As per claims 2/8, Chen further teaches wherein the step of replacing each SVT PFET with a LVT PFET includes the step of adding a LVT mask over each said SVT PFET [column 11, lines 2-18]. As per claims 3/9, Chen further teaches wherein the step of adding a LVT mask over each said SVT PFET includes the step of adding a single shape defining said LVT mask over an Nwell region to convert each said SVT PFET to said LTV PFET [column 11, lines 2-18].

Response to Arguments

Applicant's arguments filed 05/01/2006 have been fully considered but they are not persuasive.

Applicant argues against the 35 U.S.C. 102(b) rejections by Chen stating that the reference teaches the use of PFETs and NFETs having both a LVT and a SVT [Remarks page 8]. However, at column 6, lines 23-35, Chen precisely discloses the embodiment described in the specification at page 5, lines 12-31 [corresponding to figures 3A and 3B]: an AVT inverter circuit, which is by definition comprised of PFET and NFET devices connected in series, only one of which can be the LVT device, and furthermore making the considerations into a library. Therefore, given a broadest reasonable interpretation of the claimed subject matter, it is clear that Chen anticipates the claims and thus the rejections are maintained.

Applicant's arguments against the 35 U.S.C. 103(a) rejections over Jones et al. in view of Chen fail to comply with 37 CFR 1.111(b) because they amount

to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893 and e-mail is Leigh.Garbowski@uspto.gov. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER